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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,724	03/03/2004	Hyun Kyung Kim	2336-246	2634
7590 04/21/2005 ·			EXAMINER	
	TMAN GILMAN & B	DICKEY, THOMAS L		
1700 Diagonal Road, Suite 310 Alexandria, VA 22314			ART UNIT	PAPER NUMBER
1110/14114144, 11			2826	<u> </u>

DATE MAILED: 04/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)			
Office Action Summary		10/790,724	KIM, HYUN KYL	KIM, HYUN KYUNG		
		Examiner	Art Unit			
		Thomas L. Dickey	2826			
Period fo	The MAILING DATE of this communication or or Reply	appears on the cover shee	et with the correspondence a	ddress		
THE - Exte after - If the - If NC - Failt Any	ORTENED STATUTORY PERIOD FOR REI MAILING DATE OF THIS COMMUNICATION Insions of time may be available under the provisions of 37 CFR SIX (6) MONTHS from the mailing date of this communication of period for reply specified above is less than thirty (30) days, a of period for reply is specified above, the maximum statutory per ore to reply within the set or extended period for reply will, by state or period by the Office later than three months after the may or period for reply will. See 37 CFR 1.704(b).	N. 1.136(a). In no event, however, managery within the statutory minimum of will expire SIX (6) tute, cause the application to become	ay a reply be timely filed of thirty (30) days will be considered tim MONTHS from the mailing date of this ne ABANDONED (35 U.S.C. § 133).			
Status						
1)[🛛	Responsive to communication(s) filed on 25	<u> March 2005</u> .				
2a)□	This action is FINAL . 2b)⊠ T	his action is non-final.				
3)□	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.					
Disposit	ion of Claims					
5)□	Claim(s) 1-17 is/are pending in the application 4a) Of the above claim(s) 9-17 is/are withdraware Claim(s) is/are allowed. Claim(s) 1-8 is/are rejected. Claim(s) is/are objected to. Claim(s) are subject to restriction and	awn from consideration.				
Applicat	ion Papers					
•	The specification is objected to by the Exam The drawing(s) filed on <u>03 March 2004</u> is/arc Applicant may not request that any objection to the specific of th	e: a)⊠ accepted or b)□	· ,	er.		
11)	Replacement drawing sheet(s) including the corr The oath or declaration is objected to by the	•		• •		
Priority (under 35 U.S.C. § 119					
а)	Acknowledgment is made of a claim for foreign All b) Some * c) None of: 1. Certified copies of the priority docume 2. Certified copies of the priority docume 3. Copies of the certified copies of the papplication from the International Burdsee the attached detailed Office action for a least section.	ents have been received. ents have been received riority documents have b eau (PCT Rule 17.2(a)).	in Application No een received in this Nationa	ıl Stage		
Attachmen	• •	_				
1) Notice 2) Notice	e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review (PTO-948)		iew Summary (PTO-413) No(s)/Mail Date			
3) 🔲 Infor	nation Disclosure Statement(s) (PTO-1449 or PTO/SB/r r No(s)/Mail Date		of Informal Patent Application (PT	(O-152)		

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DETAILED ACTION

Election/Restriction

1. Applicant's election with traverse of Group II, claims 1-8 in the Paper filed 03/25/05 is acknowledged. Claims 1-8 and linking claims 9-11 are examined. Claims 12-17 are withdrawn.

The traversal is on the ground(s) that

The search and examination of the entire application can be made without serious burden on the Examiner ... [because] in the relevant art, i.e., semiconductor device design and fabrication, references often describe both the semiconductor device's structure and manufacturing method, as will be apparent to the Examiner upon conducting a search for prior art ... [and that t]herefore, both inventions I and II can be covered in a single search.

This is not found persuasive because in the relevant art, i.e., semiconductor device design and fabrication, references are just as likely to <u>fail</u> to describe both the semiconductor device's structure and a specific (out of several choices) method for manufacturing that structure. It is noted that applicant's traverse is premised on the somewhat pessimistic assumption that <u>all</u> claims are presently unpatentable, and that there exists a single reference that will show this. This is not necessarily going to be the case, because the product of the Group II invention could be made by a materially different process from that of the Group I invention.

The requirement is still deemed proper and is therefore made FINAL.

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Oath/Declaration

2. The oath/declaration filed on 03/03/04 is acceptable.

Drawings

3. The formal drawings filed on 03/03/04 are acceptable.

Priority

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

5. If applicant is aware of any relevant prior art, he/she requested to cite it on form **PTO-1449** in accordance with the guidelines set forth in M.P.E.P. 609.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

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A. Claims 1-5 and 8-11 are rejected under 35 U.S.C. § 102(b) as being anticipated by MAEDA ET AL. (2002/0028527).

With regard to claims 1-5 and 8 Maeda et al. discloses a wavelength converted light emitting apparatus comprising a substrate 40 having an upper surface formed with first 42 and second 43 conductive patterns, at a partial region of the first conductive pattern 42 and at the second conductive pattern 43 being formed first and second connection bumps 25, respectively; a light emitting diode 1 having first and second surfaces opposite to each other, and a side surface connected between the first and second surfaces, the first surface being formed with first 17 and second 18 electrodes, the light emitting diode 1 being disposed at the upper surface of the substrate 40 so that the first 17 and second 18 electrodes are connected to the first and second connection bumps 25, respectively; and a phosphor layer 3 formed along the second surface and side surface of the light emitting diode 1 by a certain thickness, the phosphor layer 3 serving to convert a wavelength of light emitted from the light emitting diode 1, wherein the light emitting diode 1 emits blue (note paragraph 0067) light; and the phosphor layer 3 is a material for converting the light (again, note paragraph 0067) emitted from the light emitting diode 1 into white light, the phosphor layer 3 extends from the side surface of the light emitting diode 1 so as to reach to the upper surface of the substrate 40, and the substrate 40 is a conductive and provided with a rear surface electrode 44; the first conductive pattern 42 being formed on an insulation layer 41 provided at the conductive substrate 40, and the second conductive pattern 43 being formed in a region where the

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insulation layer 41 is removed so as to be connected with the conductive substrate 40, thereby being connected to the rear surface electrode 44. Note figure 5 and paragraphs 0067 and 0093-0097 of Maeda et al.

The applicant's claims 4 and 5 do not distinguish over the Maeda et al. reference regardless of the process used to form the phosphor layer, because only the final product is relevant, not the recited processes of physical vapor deposition, chemical vapor deposition, sputtering, or spin coating.

Note that a "product by process" claim is directed to the product per se, no matter how actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

With regard to claims 9-11 Maeda et al. discloses a method of manufacturing a wavelength converted light emitting apparatus comprising the steps of: a) preparing a light emitting diode 1 having first and second surfaces opposite to each other, and a side surface connected between the first and second surfaces, the first surface being

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formed with first 17 and second 18 electrodes; b) preparing a substrate 40 having an upper surface formed with first 42 and second 43 conductive patterns, and forming first and second connection bumps 25 at a partial region of the first conductive pattern 42 and at the second conductive pattern 43, respectively; c) disposing the light emitting diode 1 at the upper surface of the substrate 40, and connecting the first 17 and second 18 electrodes of the light emitting diode 1 to the first and second connection bumps 25, respectively; and d) forming a phosphor layer 3 along the second surface and side surface of the light emitting diode 1 by a certain thickness, the phosphor layer 3 serving to convert a wavelength of light emitted from the light emitting diode 1; wherein the light emitting diode 1 emits blue (note paragraph 0067) light; and the phosphor layer 3 is a material for converting the light (again, note paragraph 0067) emitted from the light emitting diode 1 into white light, and the step d) is the step of forming the phosphor layer 3 so that the phosphor layer 3 extends along the second surface and side surface of the light emitting diode 1, and reaches the upper surface of the substrate 40 extending from the side surface of the light emitting diode 1. Note figure 5 and paragraphs 0067 and 0093-0097 of Maeda et al.

B. Claims 1 and 3-7 are rejected under 35 U.S.C.§ 102(b) as being anticipated by COLLINS ET AL. (2002/0187571).

Collins et al. discloses a wavelength converted light emitting apparatus comprising a substrate 28 having an upper surface formed with first and second conductive patterns 62 (note that first and second conductive patterns and first and second connection

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bumps are shown in detail in figure 6C, then shown as "conductive means" in figure 8A), at a partial region of the first conductive pattern 62 and at the second conductive pattern 62 being formed first and second connection bumps 52, respectively; a light emitting diode 10 having first and second surfaces opposite to each other, and a side surface connected between the first and second surfaces, the first surface being formed with first 20a and second 20b electrodes, the light emitting diode 10 being disposed at the upper surface of the substrate 28 so that the first 20a and second 20b electrodes are connected to the first and second connection bumps 52, respectively; and a phosphor layer 12 formed along the second surface and side surface of the light emitting diode 10 by a certain thickness, the phosphor layer 12 serving to convert (note paragraph 0011) a wavelength of light emitted from the light emitting diode 10, wherein the phosphor layer 12 is a material for converting the light (note paragraph 0011) emitted from the light emitting diode 10 into white light, the phosphor layer 12 extends from the side surface of the light emitting diode 10 so as to reach to the upper surface of the substrate 28, and the light emitting diode 10 further has a transparent substrate 14, first 16 and second 22 conductive semiconductor layers and an active layer 18, which are successively stacked on the transparent substrate 14 in multiple layers; the first 20a and second 20b electrodes are formed on the first 16 and second 22 conductive semiconductor layers, respectively; one surface of the transparent substrate 14 opposite to the surface formed with the first conductive semiconductor layer is provided as the second surface of the light emitting diode, and the phosphor layer 12 is formed

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along one surface of the transparent substrate 14 provided as the second surface of the light emitting diode 10, and along the side surfaces of the transparent substrate 14, the first and second conductive semiconductor layers and active layer, by a certain (30 microns plus or minus 10% max, note paragraph 0047) thickness. Note figures 3B, 6C, 8A, and paragraphs 0011, 0024, 0040-0043, and 0047 of Collins et al.

The applicant's claims 4 and 5 do not distinguish over the Collins et al. reference regardless of the process used to form the phosphor layer, because only the final product is relevant, not the recited processes of physical vapor deposition, chemical vapor deposition, sputtering, or spin coating.

Note that a "product by process" claim is directed to the product per se, no matter how actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

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Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thomas L. Dickey Patent Examiner Art Unit 2826 04/05

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